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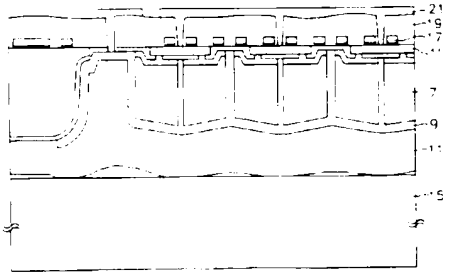
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(54) SOI transistor DRAM device and method of producing the same.

(57) A method for making a dynamic random access memory by silicon-on-insulator comprising the steps of : dividing a cell area and a peripheral area on a first silicon substrate (1) and recessing just the cell area where a memory device is formed ; forming a first insulating layer (3) by isolation of electrical elements in order to divide an active region and a passive region ; forming and patterning a first conductive layer (15) through a contact to which the active region and a capacitor are connected on the insulating layer to form a storage node ; forming a dielectric layer of the capacitor on the storage node (6) ; forming and patterning a polysilicon layer on the dielectric layer to form a storage node ; forming a second insulating layer (11) on the plate node and planarizing the insulating layer by thermal treatment ; forming a third conductive layer (13) to a predetermined thickness on the planarized insulating layer ; polishing and planarizing the third conductive layer by chemical-mechanical polishing technique using a second insulating layer as an etchstopper and bonding a second silicon substrate (15) on the planarized third conductive layer ; planarizing a backside of the first substrate by a chemical-mechanical polishing technique and exposing the active region (11) ; and forming a switching element and a bit line.

FIG.2G



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The present invention relates generally to a dynamic random access memory (DRAM) and a method for making a dynamic random access memory. More particularly, the present invention relates to a dynamic random access memory made by using a modified silicon-on-insulator (SOI) technology in which transistors are formed by silicon direct bonding (SDB) and chemical-mechanical polishing (CMP) after capacitors are formed by silicon direct bonding and the silicon-on-insulator technology. In addition, it also relates to a method for making a dynamic random access memory by which SOI devices are formed just on specific areas including cells so that the technique now applied to the bulk silicon is used for devices of peripheral circuits, with advantages of SOI direct wafer bonding.

Remarkable progress has been made in the manufacture of Dynamic Random Access Memories (DRAM) using high integration technology. As the size of semiconductor devices reduces, the problem of securing a high capacitance becomes an issue. For example, a change in main stream production from 1M bit DRAMs to 4M bit DRAMs has been achieved.

In such a DRAM with high integration, the predetermined capacitance of the cell storage capacitor must be kept constant, in spite of the decrease in the area of the cells. For example, each area of a cell and a capacitor in a 64M bit DRAM decreases to about 0.8 μm^2/1.0 μm^2.

Where the areas of charge storage capacitors are also decreased and the capacitance becomes small, soft errors may occur on exposure to α-light, and the problem of reliability becomes an issue. Accordingly, the capacitance of cell storage capacitors must be kept constant, in spite of the decrease in the areas of the capacitors, in order to obtain improved integration of a semiconductor device.

In a recent DRAM whose cells are based on transistor-stacked capacitor combinations, one of a pair of electrodes of a storage capacitor is formed to have a three-dimensional structure. This makes the capacitance larger, by 30 to 40%, than that of a two-dimensional capacitor having the same size as the three-dimensional one. However, the capacitance increases without the increase of cell areas or storage area. Various three-dimensional structures or high dielectric constant have been studied. One method for obtaining a high capacitance in defined small areas of capacitors, such as the above three-dimensional DRAMs is described in "A 1.28μm Bit-Line Shielded Memory Cell Technology for 64 MB DRAMS" - 1990 symposium of VLSI TECHNOLOGY.

Active parasitic devices arise such as parasitic metal oxide semiconductor transistors or parasitic bipolar transistors in a PN junction-separation structure that appears in a complementary metal oxide semiconductor structure. In addition, problems can occur of deterioration of electric devices and soft error due to latch-up phenomenon. In order to prevent these problems and attain high density, silicon-on-insulator (SOI) techniques have been studied in which insulating layers are formed as sidewalls of an insulating substrate formed of a material such as Si02 and silicon single crystalline wells are formed in these insulating layers to form semiconductor devices in the above wells.

These techniques have advantages of perfect isolation of electrical elements, high speed performance, and being latch-up and soft error free. That is, a semiconductor device such as CMOS circuits can be made. Second, the width of insulating layers for isolation depends on just photo-etching, etc. Third, high integration based on the micro-miniaturization can be obtained as well as the application with three-dimensional devices.

According to the above techniques, a semiconductor device of SOI structure is formed by forming an amorphous or polysilicon layer on an amorphous insulating substrate such as SiO_2 and performing recrystallization on the polysilicon layer. Separation by implanted oxygen (SIMOX) processes and full isolation by porous oxidized silicon (FIPOS) processes are also known, as another approach.

When it comes to the problems of these SIMOX technologies, specially designed oxide ion implanting means are required for forming an insulating layer inside a substrate. The FIPOS processes need anodization just for these processes. Also, zone melting (ZMR) requires recrystallization.

A method of forming a conventional DRAM is now described with reference to FIG. 1.

First, a field oxide layer 2 is formed by selective oxidation on a silicon substrate 1 and isolation of electrical elements is performed. Then, a gate oxide 8 is grown, and a gate electrode 17 is patterned to form a source/drain region. Inter layer insulation is carried out by an oxide layer 19 formed by chemical vapour deposition method, and a conductive layer 21 is deposited and patterned.

After a second interlayer insulation is carried out, a contact hole is opened so that a capacitor lower electrode 7 contacts the first silicon substrate, and the lower electrode 7 is patterned. A dielectric layer 10 and an upper electrode 9 are then formed.

Successively, after a third interlayer insulation is performed, a protective layer 25 is finally formed to complete the manufacture of the semiconductor memory cell.

As shown in the above process, in order to attain sufficient capacitance in the manufacture of the high integration DRAM more than the level of very large scale integrated circuits (VLSI), a stack type capacitor having a three-dimensionally enlarged area is applied.

As the integrity of the stack type capacitor is more than 64M, a storage node is formed in order to secure

the capacitance of the cell capacitor. If the storage node is raised so that there is a large step difference between a cell part and a peripheral part, then contact or metallization is not easily performed.

In the formation of P-MOS transistors, there is a condition that thermal budget should be small in order to maintain transistor characteristics and isolation of electrical elements. It is hard to perform planarization by borophosphorsilicate glass (BPSG) flow due to this condition.

In line with the high integration of DRAMs, the degree of difficulty of forming patterns increases. This is not only because the size of patterns is small but because high overlay accuracy is necessary, and since there is a step-like difference as high as the height of the cell capacitor, it is difficult to secure an alignment margin.

If the planarity is increased so as to remove the step-like difference, the depth of contact for metallization is increased, too. Various problems may occur by step-coverage or etch damage.

Study has been made to attempt to solve the problems by forming a capacitor in advance by direct wafer bonding and silicon-on-insulator processes and then making transistors on the opposite silicon surface.

However, if a DRAM cell is made by this way, devices of peripheral circuits become SOI devices, and it is difficult to find a processing condition that meets both characteristics.

That is to say, n-type MOS and p-type MOS transistors having a width and a length different to each other should be made into SOI devices, and there is a difficulty forming active devices of different size on SOI.

An object of this invention is to provide a dynamic random access memory and a method for making the same, which is capable of preventing deterioration to characteristics of a transistor due to subsequent thermal treatment and problems of grounding plate, by forming the transistor after a cell area is deeply recessed on a semiconductor substrate having the cell area and a peripheral area, and a capacitor is formed.

A second object of this invention is to provide a method for making a dynamic random access memory using silicon-on-insulator so as to maintain the advantages of direct wafer bonding (DWB) and silicon-on-insulator (SOI) techniques and to apply the technique applied to the bulk silicon, directly to the devices of the peripheral circuit. This object can be achieved by forming just an access transistor in a cell area on a silicon-on-insulator of less than 100μm and forming devices other than the access transistor on a silicon-on-insulator of more than 1μm so as to display characteristics of devices formed on the bulk silicon.

In a first aspect, a method for making a dynamic random access memory by silicon-on-insulator comprises the steps of:-

dividing a cell area and a peripheral area on a first silicon substrate and recessing just the cell area where a memory device is formed;

forming a first insulating layer by isolation of electrical elements in order to divide an active region and a passive region;

forming and patterning a first conductive layer through a contact to which the active region and a capacitor are connected on the insulating layer to form a storage node;

forming a dielectric layer of the capacitor on the storage node;

forming and patterning a polysilicon layer on the dielectric layer to form a storage node;

forming a second insulating layer on the plate node and planarizing the insulating layer by thermal treatment;

forming a third conductive layer to a predetermined thickness on the planarized insulating layer;

polishing and planarizing the third conductive layer by chemical-mechanical polishing technique, using the second insulating layer as an etchstopper and bonding a second silicon substrate on the planarized third conductive layer;

planarizing a back side of the first substrate by a chemical-mechanical polishing technique and exposing the active region; and

forming a switching element on the forming a bit line.

A dynamic random access memory made by siliconon-insulator according to the invention comprises:

an active silicon layer formed to be divided into several parts, separated from each other by chemically and mechanically polishing and planarizing a back side of a first substrate having a recessed cell area where a memory device will be formed;

a first insulating layer formed to be divided into an active region and a passive region on the active silicon layer;

a storage node formed on right and left sides of a contact on the first insulating layer;

a plate node formed on the storage node;

a second insulating layer formed on the plate node;

a handling wafer bonded to a pattern of a polysilicon layer deposited on the second insulating layer and polished chemically and mechanically and planarized;

a gate electrode formed on the active silicon layer;

a third insulating layer formed to be divided into several parts and separated from each other on the active silicon layer where the gate electrode is formed; and

a bit line formed on the third insulating layer.

In accordance with a further aspect of this inven-

tion, a method for making a dynamic random access memory by silicon-on-insulator comprises the steps of:

recessing a specified area including a dynamic random access memory cell formed on a silicon substrate;

forming a well on the substrate;

forming a trench in order to isolate electrical elements between cells in the recessed area and form an align-key;

filling the trench with buried oxide;

forming a buried contact on the buried oxide;

forming a capacitor;

planarizing a pattern formed by the processes;

bonding an active wafer passed the processes to a handle wafer;

removing a silicon of the active wafer to a bottom of the trench;

wet-etching a silicon layer formed on an area that is not recessed on the silicon substrate and performing isolation of electrical elements by means of a local oxidation of silicon process;

forming devices of a peripheral circuit such as n-type and p-type metal oxide semiconductors and a register pattern in a conventional manner;

forming devices such as a metal oxide semiconductor and a transistor on the recessed area of the silicon substrate;

forming contacts simultaneously on a plate node, a cell, a gate and a metallization of the peripheral circuit and on a bit line, respectively;

forming simultaneously a bit line of the cell area and the metallization of the peripheral circuit; and

carrying out passivation and alloying on the pattern.

The above and further objects, features and advantages of the present invention will become more apparent from the following detailed description of embodiments taken in conjunction with the accompanying drawings.

FIG. 1 is a sectional view of a conventional dynamic random access memory (DRAM);

FIGS. 2A to 2G depict the steps in the manufacture of a DRAM by silicon-on-insulator processes in accordance with a first preferred embodiment of this invention;

FIGS. 3A to 3I depict the steps in the manufacture of a DRAM by silicon-on-insulator processes in accordance with a second preferred embodiment of this invention;

FIG. 4 depicts a joining machine that is used at the time of manufacturing the DRAM in accordance with the second preferred embodiment of this invention.

A detailed description of the present invention will now be made referring to the accompanying drawings.

A first preferred embodiment of making a dynamic random access memory (DRAM) by silicon-on-insulator (SOI) techniques is described as follows.

FIGS. 2A to 2G depict the steps in the manufacture of a DRAM by silicon-on-insulator processes in accordance with a first preferred embodiment of this invention.

The method of manufacturing a dynamic random access memory (DRAM) includes the steps of dividing a cell part and a peripheral part on a first single crystalline silicon substrate 1 and recessing deeply just the cell part where a memory device is formed; forming a first insulating layer 3 by isolation to separate an active region and a passive region; forming and patterning first conductive polysilicon layers 5, 7 on the insulating layer 3 through a contact to which the active region and capacitor are connected to form a storage node 6; forming and patterning a capacitor dielectric layer and a polysilicon layer on the storage node 6 to form a plate node 9; forming and thermally treating a second insulating layer 11 on the plate node 9 to be planarized; forming another polysilicon layer 13 to a predetermined thickness on the planarized second insulating layer 11; polishing the polysilicon layer chemically and mechanically, using the second insulating layer as an etchstopper and bonding a handling wafer 15 on the polished first substrate; thinning a backside part of the first substrate 1 by a chemical-mechanical polishing method to expose an active silicon layer 1'; and after making a gate electrode 17 on the active silicon layer 1' and a predetermined device, applying a third insulating layer 19 and forming a bit line 21.

To explain the above processes in detail, the cell part where a memory device is deeply recessed after the cell part and the peripheral part are divided on the single-crystalline silicon substrate 1, as shown in FIG. 2A.

The cell part is recessed more than the height of the capacitor. After just the part that will be isolated in the recessed cell part is etched to a thickness of more than 500 angstroms by shallow trench technique, an oxide layer is formed for damage cure, and a high temperature oxide (HTO) and a borophosphorsilicate glass (BPSG) are united with each other to form an insulating layer 3 to a thickness in which can be isolated.

A first conductive layer of polysilicon is formed on the insulating layer 3 so thickly that sufficient capacitance can be obtained through the contact to which the active region and capacitor are connected. After patterning the first conductive layer, the storage node 6 is formed. The first conductive layer is deposited by a differential doped polysilicon deposition that forms a doped polysilicon layer 7 thickly, after an undoped polysilicon layer 5 is thinly formed. When a junction of the source region is formed by a successive thermal treatment after the capacitor processes,

the above way prevents the junction from being formed too deeply. The first conductive layer is patterned to form the storage node 6.

Dielectric layers of the capacitor are formed by various high dielectric materials such as oxide film/nitride film/oxide film that does not appear on the pattern where the storage node 6 is formed as shown in FIG. 2D. The second conductive layer, polysilicon is formed and patterned to form a plate node 9 thereby completing the capacitor processes.

After the insulating layer to which HTO and BPSG are united is thickly formed and planarized by thermal treatment, the polysilicon layer 13 is formed to a predetermined thickness.

As shown in FIG. 2E, the polysilicon layer 13 is planarized by CMP method in which the insulating layer 11 serves as an etch stopper, and a glass side of the handling wafer 15 is bonded on the planarized polysilicon layer. The bonding method is similar to a conventional way, i.e. the bonding is performed by thermal treatment.

Referring now to FIG. 2F, being turned upside down, the backside of the wafer where the capacitors are formed is polished by CMP method using the insulating layer 3 as an etch stopper.

Successively, as shown in FIG. 2G, the gate electrode 17 is formed on the active silicon layer 1' remained after the CMP process, and the source/drain region is made by ion-implantation to form the switching elements. After that, the insulating layer 19 is applied and the bit line 21 is formed.

The above-mentioned contact is formed on the borderline between the cell part and the peripheral part to be connected with the plate node 9, the second conductive layer of the capacitor formed in the opposite side. The plate node 9 can be grounded after the insulating layer 3 formed in the field area and the dielectric layer for the capacitor are removed completely.

After the metallization and passivation processes, the processes of the memory cell are completed.

A second preferred embodiment of the DRAM by using SOI technology is described as follows.

FIGS. 3A to 3I depict the steps in the manufacture of a DRAM by silicon-on-insulator processes in accordance with a second preferred embodiment of this invention. FIG. 4 depicts a joining machine that is used at the time of manufacturing the DRAM in accordance with the second preferred embodiment of this invention.

In the processes for making a DRAM in accordance with the second preferred embodiment of this invention, access transistors of cell areas are formed on SOI having a thickness of less than 100 nm. Another devices except the access transistors are formed on SOI having a thickness of 1μm so as to display the characteristics of the devices formed on a bulk silicon.

The processes therefor include a first step for recessing certain areas including the parts where DRAM cells are formed on a silicon substrate 100; a second step for forming wells on the substrate; a third step for forming a trench 104 to isolate electrical elements between cells and form align-keys on the recessed area; a fourth step for filling the trench 104 with a buried oxide 106; a fifth step for forming a buried contact 108 on the buried oxide 106; a sixth step for forming capacitors; a seventh step for planarizing a pattern formed through the above steps; an eighth step for cutting an active wafer on which the above steps are carried out to join it to a handle wafer 112; a ninth step for recessing the silicon of the active wafer nearly to the bottom of the trench formed in the third step; a tenth step for wet-etching the silicon formed on the area that is not recessed in the first step and isolating electrical elements by a local oxidation of silicon (LOCOS) process; an eleventh step for forming devices of peripheral circuits such as n-type MOS and p-type MOS transistors and register patterns after the above processes; a twelfth step for forming MOS transistors on the recessed area of the silicon substrate; a thirteenth step for forming simultaneously contacts and bit-line contacts on a plate node, a cell, gate electrodes of a peripheral circuit and a line of the peripheral circuit; a fourteenth step for forming a bit line of the cell area and a line of the peripheral circuit; and a fifteenth step for carrying out passivation and alloying on the pattern after the above steps.

The above steps are now in detail described with reference to the drawings.

As a first step, boron and Ge are ion-implanted by a high energy of 1E20/cm^2 on a bare silicon 100, and when the active wafer is thinned at the later process, an etchstopper layer 102 that can be used as an etchstopper is formed. After direct wafer bonding (DWB) treatment, the silicon of the area where a thin SOI is formed is wet-etched to a thickness of l and recessed. Recessing the oxide layer after local oxidation instead of the wet etching may be available but it has a difficulty of recessing the oxide layer to a depth of more than 1μm. The recess by wet-etching the silicon has a problem of uniformity of recessed depth. Therefore, boron and Ge are ion-implanted by a high energy of 1E20/cm^2 to use an etchstopper at the time of the recess. In this case, two etchstop layers 102 whose thicknesses differ from each other's.

The p-type well and n-type well are respectively formed by ion-implantation of boron and phosphorous in the second step.

The third step uses a thermal oxide layer of more than 30nm as a mask of the trench etching. The depth of the trench is over 150nm and below 300 nm, and patterning is carried out so that the area where electrical elements are isolated, the region where a contact of a plate node 116 is formed, and the align-key neces-

sary for the sixth step. After the formation of the trench 104, boron or BF_2 is ion-implanted for doping the element-isolated area, and the oxide layer serving as the mask is removed.

After the thermal oxide layer is grown to a thickness of 10nm, and an oxide layer by CVD is applied thereto thickly more than the depth of the trench, a silicon nitride layer of 10nm is deposited, and an oxide layer by CVD is deposited thereby making the state of FIG. 3B. The reason why the silicon nitride layer is inserted between the oxide layers is that a plate poly 120 is
deposited between the storage node 118 and the buried oxide 106 (silicon oxide layer/silicon nitride layer) thereby increasing the capacitance of the capacitor and the SOI serves as a back gate.

In the fifth step, the buried contact 108 is formed on the buried oxide 106 (thermal oxide + HTO + SiN + HTO), and this contact 108 connects the storage node to the thin SOI. Phosphorous is ion-implanted to the above contact.

The capacitor formed in the sixth step has a cylindrical shape or a crown shape in accordance with the design rule, required stored capacitance, etc. After insitu phosphorous doped poly silicon is applied to a thickness of more 200 nm than the depth of the recess in order that the planarity is good at the time of patterning the storage node 118 and the align-key formed in the third step is exposed, the storage node is patterned by CMP method. The oxide layer is wet-etched provided the oxide layer applied in the fourth step is exposed by dry-etching the storage poly 114, The silicon nitride layer formed in the fourth step serves as a stopping layer of the etching. When silicon nitride layer/oxide layer (NO) dielectric layer is formed and insitu- doped poly is applied, the plate poly 116 is applied between the storage node 118 and buried oxide, as shown in a circle A of FIG. 3D. The plate poly 116 is applied to a thickness of 100 to 200 and patterned to have a configuration of FIG. 3D.

The seventh step is a step for polishing global topology and undulated surface so that DWB process is possible. The oxide layer by CVD and a borophosphorsilicate glass (BPSG) 122 are applied and reflow is carried out at a temperature of more than 800°C. Polysilicon 124 is applied and the CMP process is carried out to form the configuration of FIG. 3E. The BPSG 122 serves as a stopping layer of this CMP process. The oxide layer by CVD (including the BPSG 122) is overlaid and thermal treatment is carried out to complete the planarization.

The eighth step is a step for joining the handle wafer 112
and the active wafer formed through the 7th step, and includes the following three stages. As a first stage, the active wafer and the handle wafer that will be joined together are dipped respectively in a mixed solution of sulfuric acid and aqueous hydrogenperoxide of 130°C and a mixed solution of liquid ammonia and aqueous hydrogenperoxide of 80°C for a few minutes. The two wafers are dried and their particles are then removed such that their surfaces are terminated to an alkali radical.

As a second stage, two wafers join the joining machine shown in FIG. 4, with the planarized surface of the active wafer facing the glass side of the handle wafer.

The following table 1 shows that misalignment of the rotational direction may be controlled at an angle of less than 0.01 if the wafers are joined together by using the joining machine. Big misalignment causes a problem of alignment in the photoetching process after the tenth step.

As a third stage, two wafers are thermally treated for more than two hours in an ambient of nitrogen at a temperature of over 800°C, and, successively, a thermal oxide layer is then formed in an ambient of oxygen in order to increase joining intensity
and remove voids of the joining interface. Forming the thermal oxide layer can prevent the handle wafer from being damaged at the time of wet-etching the silicon.

Table 1:

The Result of Gauging the Misalignment of the Rotational Direction After the Joining of the Two Wafers	
Sample No.	Measured Degree
1	0.008°
2	0.008°
3	0.001°

In the next 9th step, the active wafer passes through a series of backlapping/wet-etching/CMP. The backlapping is used for the purpose of enhancing the throughput, since the speed of removing the silicon just by CMP is too slow. The wet-etching removes silicon particles produced by the backlapping to decrease occurrence of scatches and deterioration of the wafer in the subsequent CMP process and uniform the thickness of the silicon layer by using an etchstopper. The silicon layer is thinned to a thickness of 50μm by the backlapping, and is then thinned to several micro-meters by means of a mixed solution of KOH/IPA of about 80°C in the wet-etching. The remained silicon is thinned by CMP. The oxide layer filled in the trench in the fourth step serves as a polish stopper, as shown in FIG. 3G.

Referring now to the tenth step, the thin SOI area, i.e. the recessed area is covered with a silicon oxide

layer/silicon nitride layer/silicon oxide layer. The silicon in the thick SOI area is wet-etched to form a step-like difference of about 300nm between the thin SOI area and the thick SOI area. After that, isolation of electrical elements is performed in the thick SOI area by LOCOS. The oxide layer formed on the nitride layer in the thin SOI area is removed under the etching process of the oxide layer, and the nitride layer and the oxide layer formed underneath the nitride layer are remained. In the eleventh step, after n-type and p-type MOS transistors, register patterns, etc. are formed, an oxide layer formed by CVD is applied thereto such that it is higher than the top of the silicon nitride layer remained in the thick SOI area by about 200nm. The CVD oxide layer is planarized by CMP, by using the nitride layer as a stopper. The nitride layer and the oxide layer are wet-etched to have a configuration as shown in FIG. 3H.

In the twelfth step, a thermal oxide layer of 50 nm is formed. An oxide layer is formed to a thickness of more than 150nm in the region having the phosphorous out-diffused in the storage node 118 formed in the sixth step after the ion-implantation in the fifth step. The oxide layer of 60nm is wet-etched and the gate oxide layer is again formed. Gate electrodes I, II 124, 124' are then formed, and source/drain is formed to form SOI transistor. The gate electrode 124 is formed of metal, e.g. W or composite of Ti nitride layer and metal, and then patterned to be a line of thick SOI region simultaneously with patterning the gate line. After that, a CVD oxide layer is applied as an interlayer insulating layer.

In the thirteenth step, a contact and a bit line contact are simultaneously formed over the plate node 116, cell, gate electrode of the peripheral circuit, metallization of the peripheral circuit.

Referring now to FIG. 14, the bit-line 127 is formed on the pattern where the contact is formed. The bit-line is formed of metal, and is patterned simultaneously with the line of the thick SOI region to have a structure of FIG. 3I. The reference numerals appearing in the drawing designate the following elements: ONO 110; an oxide layer 125; a bonded interface 128; and SiO_2 129. When it comes to the fifteenth step, customary semiconductor manufacturing processes such as passivation and alloying are carried out on the pattern to complete a DRAM.

In the first preferred embodiment of this invention, even if the storage node is raised to secure the capacitance of the capacitor at the time of manufacturing a DRAM, there is no problem of step-like difference between the peripheral area and the area. Besides, even if the device is highly integrated, the area where one capacitor occupies is relatively small but the height may be increased as much as you like, and the sufficient capacitance of the capacitor can be secured. Since the processes for manufacturing the DRAM begin with forming the capacitor and the transistor is then formed, there can be prevented the deterioration to the characteristic of the transistor due to the weak of the junction caused by the subsequent thermal treatment. Thus, the subsequent processes may be easily carried out. Since the cell area is recessed by the shallow trench method, a thick oxide layer is not used at the time of the isolation of electrical elements to facilitate the formation of the contact for grounding the plate node of the capacitor on the borderline of the peripheral area and the cell area. Referring to the second preferred embodiment, the advantages of DWB and SOI techniques are maintained intact by forming the SOI devices just in the specified areas including the cell area, and there can be solved problems such as step coverage and etch damage caused by increasing the planarity to overcome the step-like difference of the capacitor. The technique applied to the bulk silicon may be directly to the devices of the peripheral circuit.

Claims

1. A method for making a dynamic random access memory by silicon-on-insulator comprising the steps of: dividing a cell area and a peripheral area on a first silicon substrate (1) and recessing just said cell area where a memory device is formed; forming a first insulating layer (3) by isolation of electrical elements in order to divide an active region and a passive region; forming and patterning a first conductive layer (5) through a contact to which said active region and a capacitor are connected on said insulating layer to form a storage node; forming a dielectric layer of the capacitor on said storage node (6); forming and patterning a polysilicon layer on said dielectric layer to form a storage node; forming a second insulating layer (11) on said plate node and planarizing said insulating layer by thermal treatment; forming a third conductive layer (13) to a predetermined thickness on said planarized insulating layer; polishing and planarizing said third conductive layer by a chemical-mechanical polishing technique, using said second insulating layer as an etchstopper and bonding a second silicon substrate (15) on said planarized third conductive layer; planarizing an opposite side of the first substrate by a chemical-mechanical polishing technique and exposing said active region (11); forming a switching element on said active region, forming a third insulating layer (19) and then forming a bit line (21).

2. The method according to Claim 1, wherein said first insulating layer is formed of a high temperature oxide layer and/or a borophosphorsilicate glass layer.

3. The method according to Claim 1 or Claim 2, wherein said first conductive layer is formed by a differential doped polysilicon deposition method forming an undoped polysilicon layer (7) thinly and forming a doped polysilicon layer thickly on said undoped polysilicon layer.

4. The method according to any preceding claim, wherein said second insulating layer is combined with high temperature oxide and borophosphorsilicate glass.

5. The method according to any preceding claim, wherein said bit line is formed to be connected with the plate node, the second conductive layer formed on the opposite side through the contact on a border line between the peripheral area and the cell.

6. The method according to Claim 5, wherein a plate poly is grounded after removing completely the insulating layer formed in a field and the first insulating layer, a dielectric layer of capacitor.

7. The method according to any preceding claim, wherein said third conductive layer is formed of polysilicon.

8. The method according to any preceding claim, wherein said active region is formed of an active silicon layer.

9. A dynamic random access memory made by siliconon-insulator, comprising: an active silicon layer (1) formed to be divided into several parts and separated from each other by chemically and mechanically polishing and planarizing the back of a first substrate having a recessed cell area where a memory device will be formed; a first insulating layer (3) formed to be divided into an active region and a passive region on said active silicon layer; a storage node (6) formed on sides of a contact on said first insulating layer; a plate node (9) formed on said storage node; a second insulating layer (11) formed on said plate node; a handling wafer (15) bonded to a pattern of a polysilicon layer deposited on said second insulating layer and polished chemically and mechanically and planarized; a gate electrode (17) formed on said active silicon layer; a third insulating layer (19) formed to be divided into several parts and separated from each other on the active silicon layer where said gate electrode is formed; and a bit line (21) formed on said third insulating layer.

10. A method for making a dynamic random access memory by silicon-on-insulator comprising the steps of:

recessing a specified area including a dynamic random access memory cell formed on a silicon substrate (100); forming a well on said substrate; forming a trench (104) in order to isolate electrical elements between cells in said recessed area and form an align-key; filling said trench with buried oxide (105); forming a buried contact (108) on said buried oxide; forming a capacitor; planarizing a pattern formed by said processes; bonding an active wafer passed said processes to a handle wafer (112); removing silicon of said active wafer to a bottom of said trench; wet-etching a silicon layer formed on an area that is not recessed on said silicon substrate and performing isolation of electrical elements by means of a local oxidation of silicon process; forming devices of a peripheral circuit such as n-type and p-type metal oxide semiconductors and a register pattern in a conventional manner; forming devices such as a metal oxide semiconductor and a transistor on the recessed area of said silicon substrate; forming contacts simultaneously on a plate node, a cell, a gate and a metallization of the peripheral circuit and on a bit line, respectively; forming simultaneously a bit line (127) of the cell area and the metallization of the peripheral circuit; and carrying out passivation and alloying on said pattern.

11. The method according to Claim 10, wherein recessing the silicon of said active wafer to a bottom of said trench follows lapping/wet-etching/chemical-and-mechanical polishing.

12. The method according to Claim 10 or 11, wherein an etchstopping layer is formed so as to facilitate said lapping/wet-etching/chemical-and-mechanical polishing process prior to recessing the specified area.

13. The method according to any one of Claims 10 to 12, wherein an etchstopping layer is formed so as to facilitate recessing the specified area prior to said process.

14. The method according to any one of Claims 10 to 13, wherein said planarization process includes a chemical-and-mechanical polishing process after applying a buried oxide and overlaying polysilicon or amorphous silicon.

15. The method according to any one of Claims 10 to 14, wherein said active wafer is bonded to a handling wafer after an SiO_2 layer is formed.

16. The method according to any one of Claims 10 to 15, wherein the bonding process of said active wafer and handling wafer is carried out by suc-

cessively and thermally treating in an ambient of 0_2 after thermal treatment in an ambient of N_2.

17. The method according to any one of Claims 10 to 16, wherein a gate electrode of said metal oxide semiconductor in the cell area and the line of the peripheral circuit are simultaneously formed.

18. The method according to any one of Claims 10 to 17, wherein isolation of electrical elements using a local oxidation of silicon process is performed by making devices of the peripheral area and applying an interlayer insulating layer after covering a silicon oxide layer/silicon nitride layer/silicon oxide layer on a specified area including the cell, and then carrying out a planarization in a chemical-mechanical polishing method, using the silicon nitride layer of a predetermined area as a stopper.

19. The method according to any one of Claims 10 to 18, wherein said process for making the capacitor a plate node of said capacitor penetrates between the buried oxide and the storage node.

FIG. 1

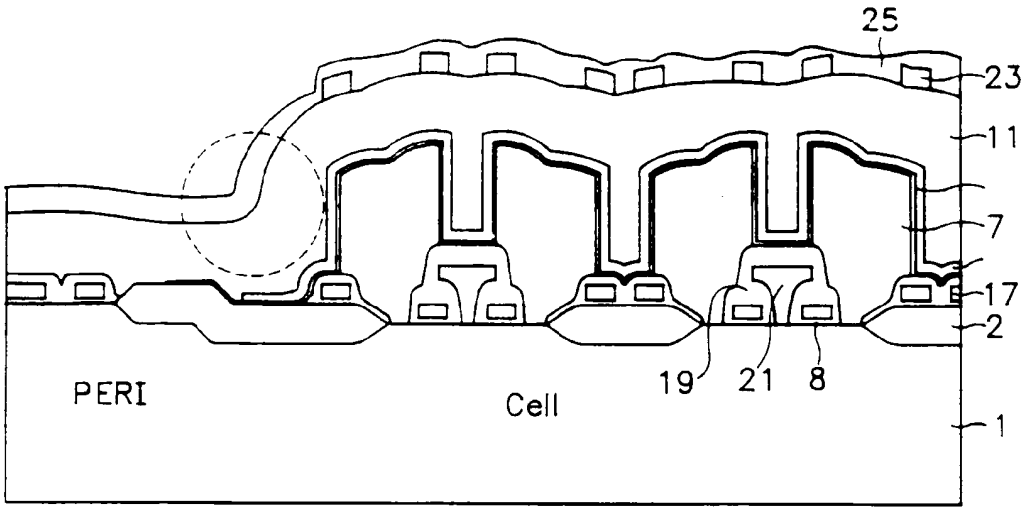


FIG. 2A

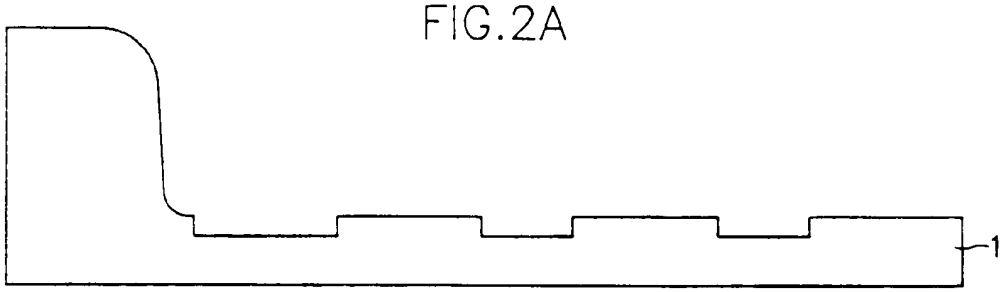


FIG. 2B

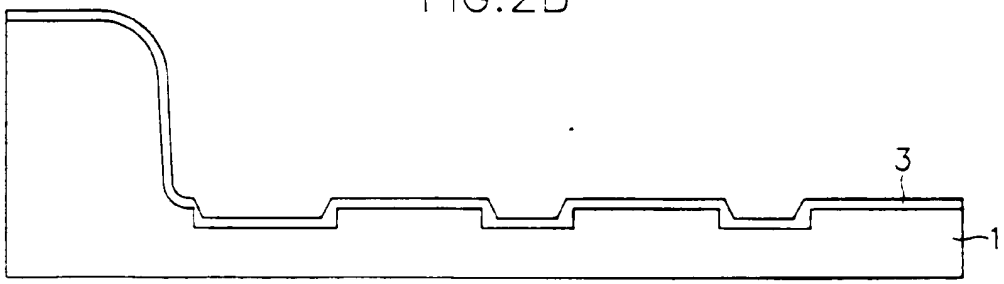


FIG. 2C

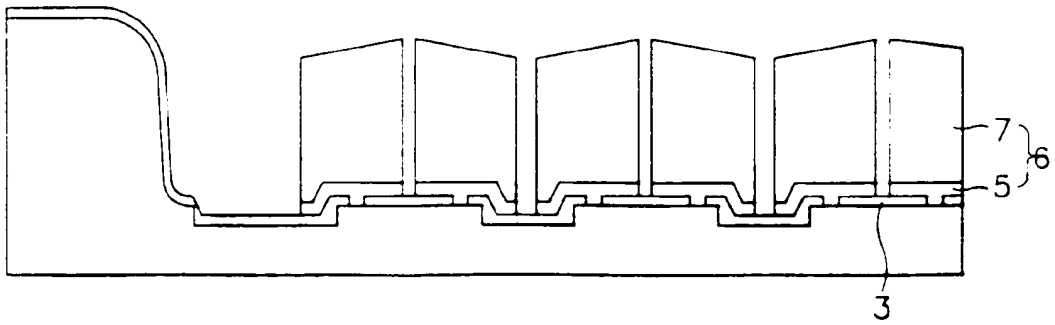


FIG.2D

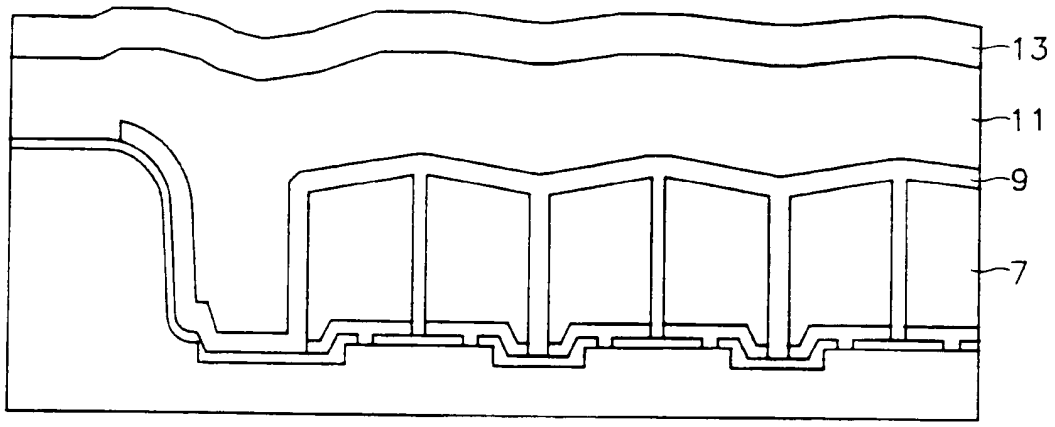


FIG.2E

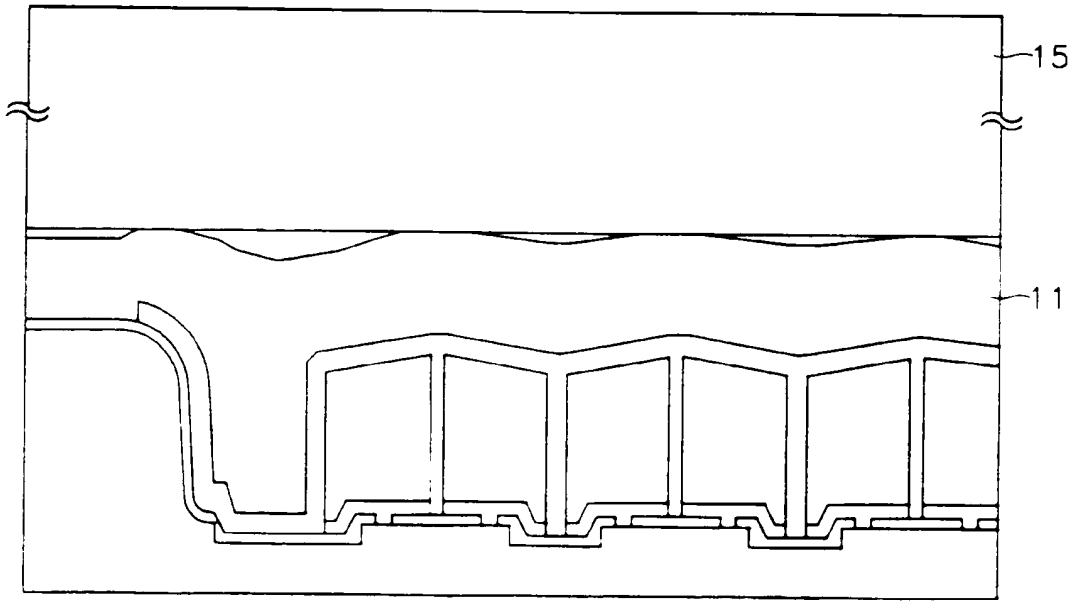


FIG.2F

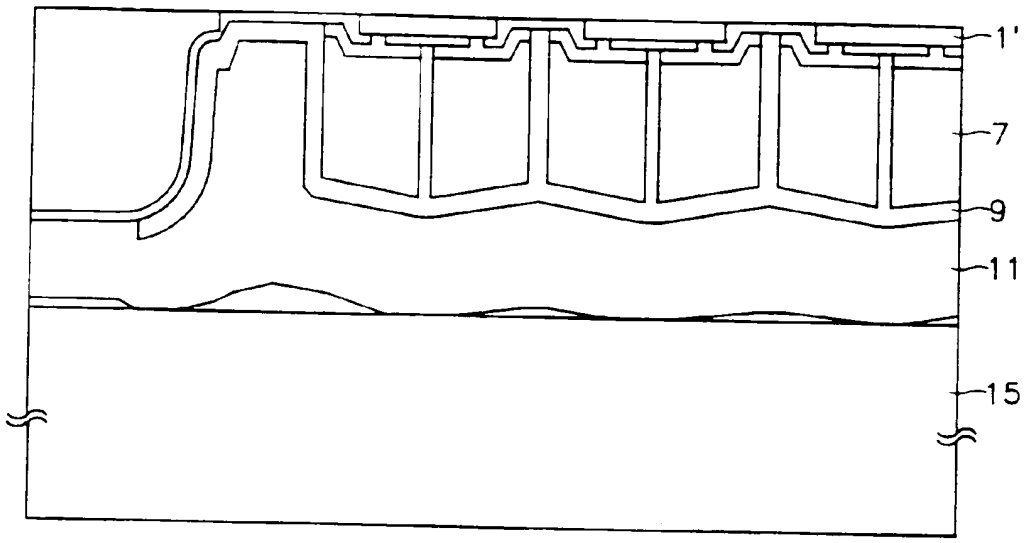


FIG.2G

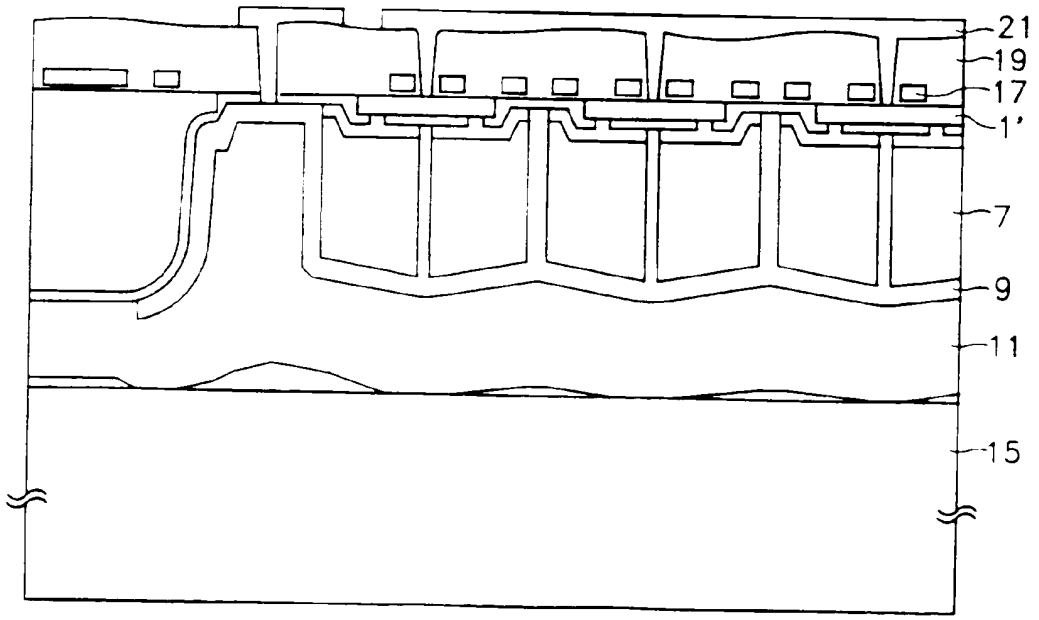


FIG.3A

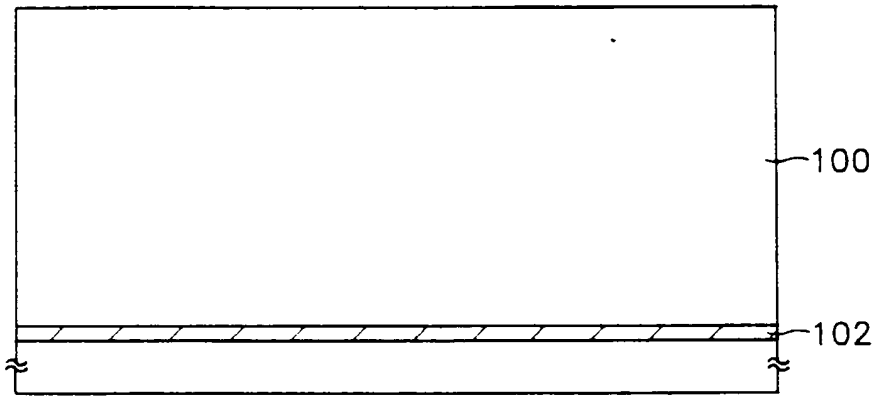


FIG.3B

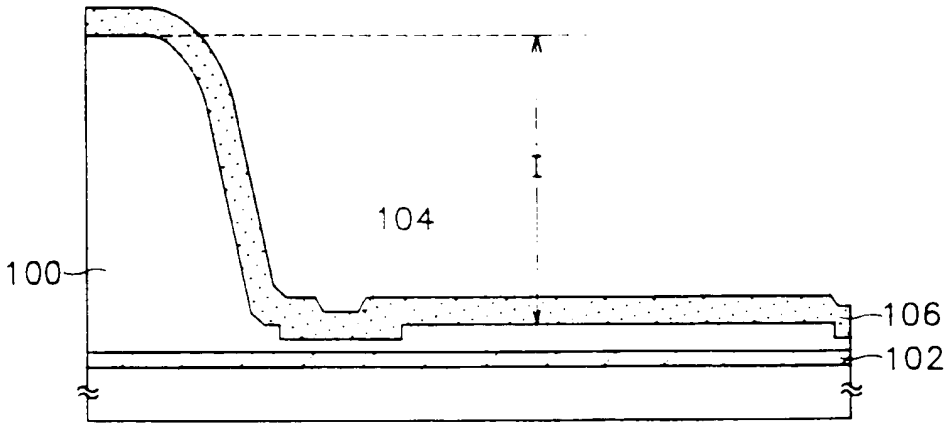


FIG.3C

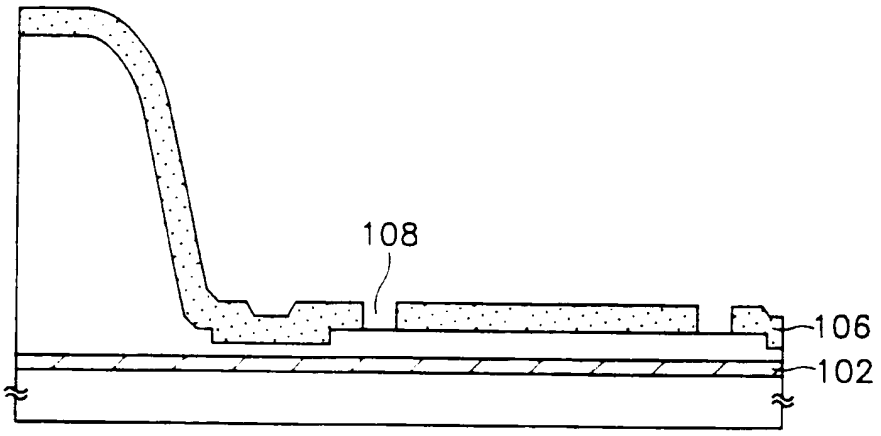


FIG.3D

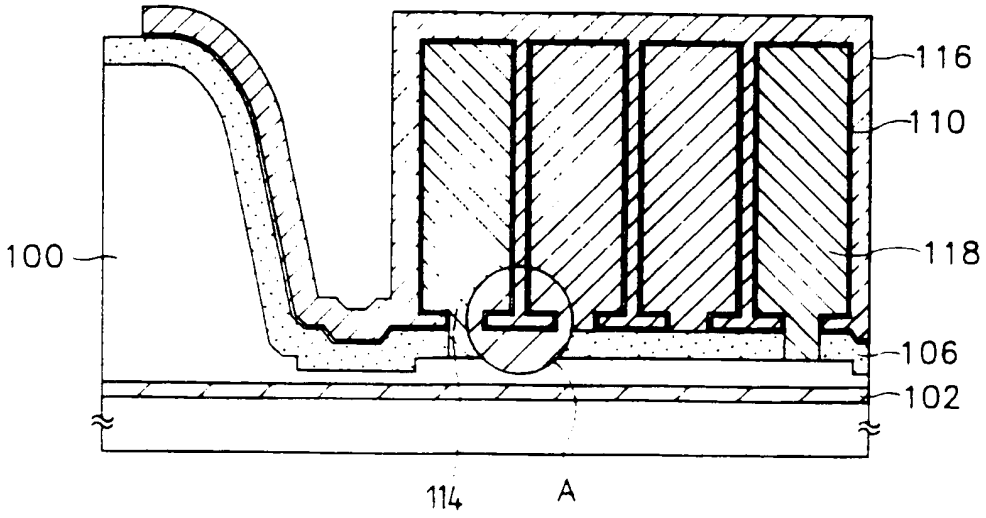


FIG.3E

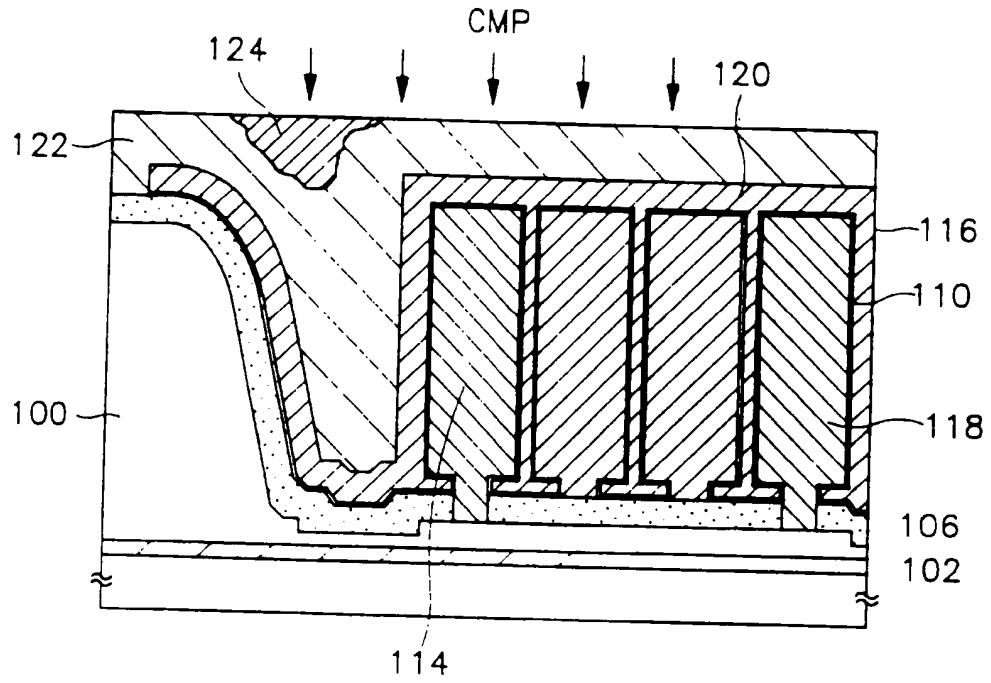

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FIG.3F

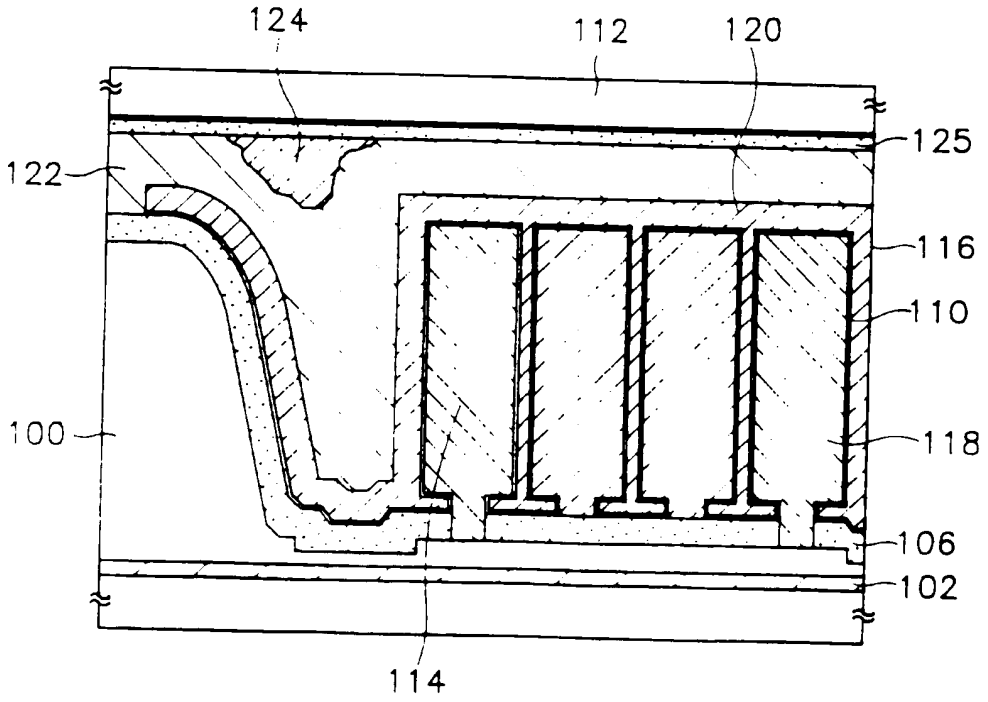

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FIG.3G

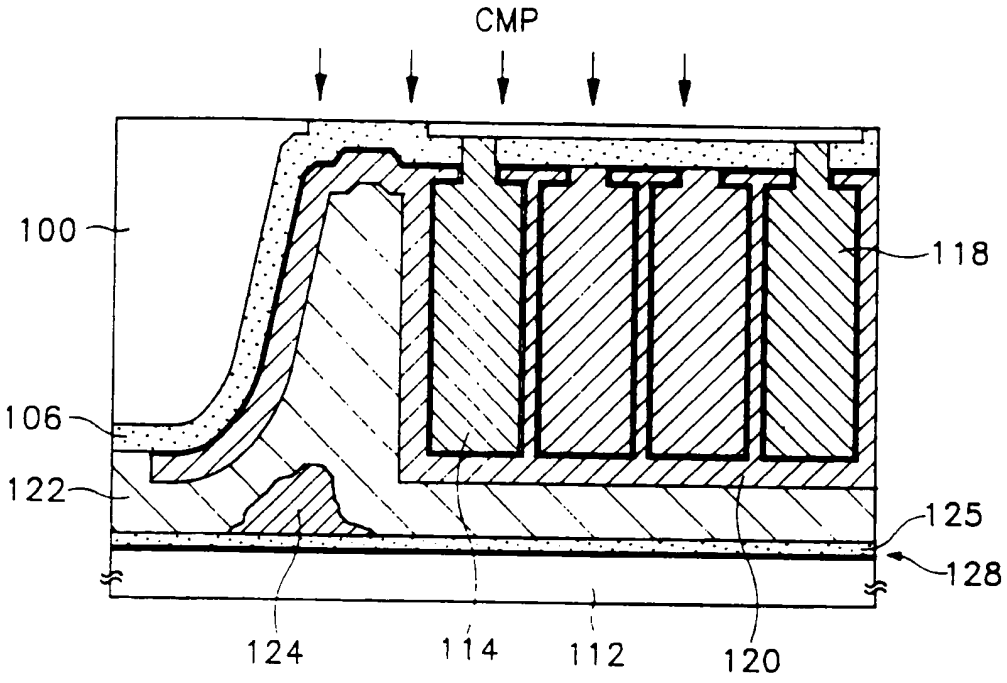

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FIG.3H

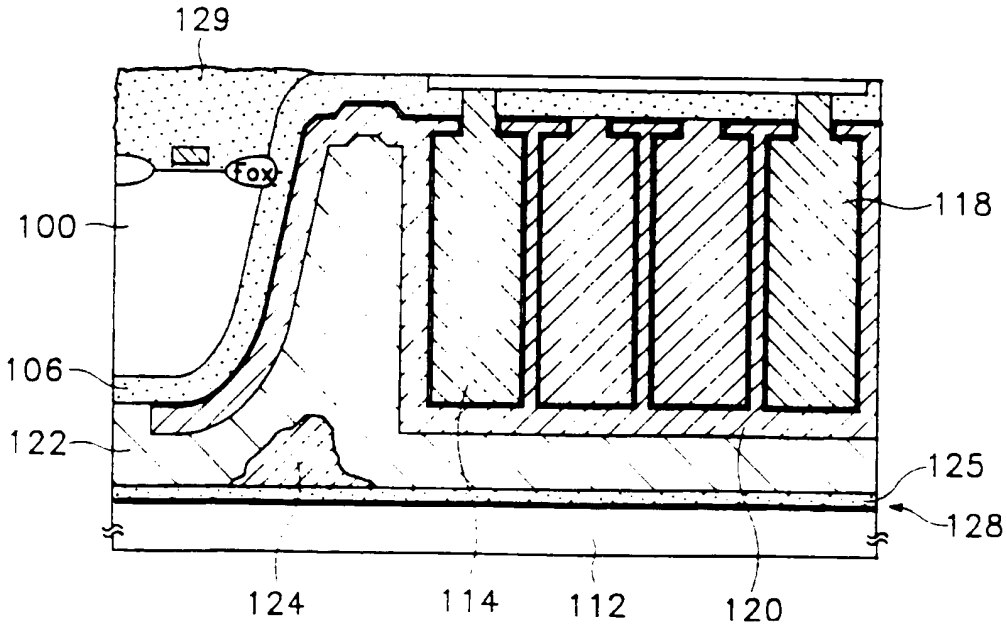

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FIG.31

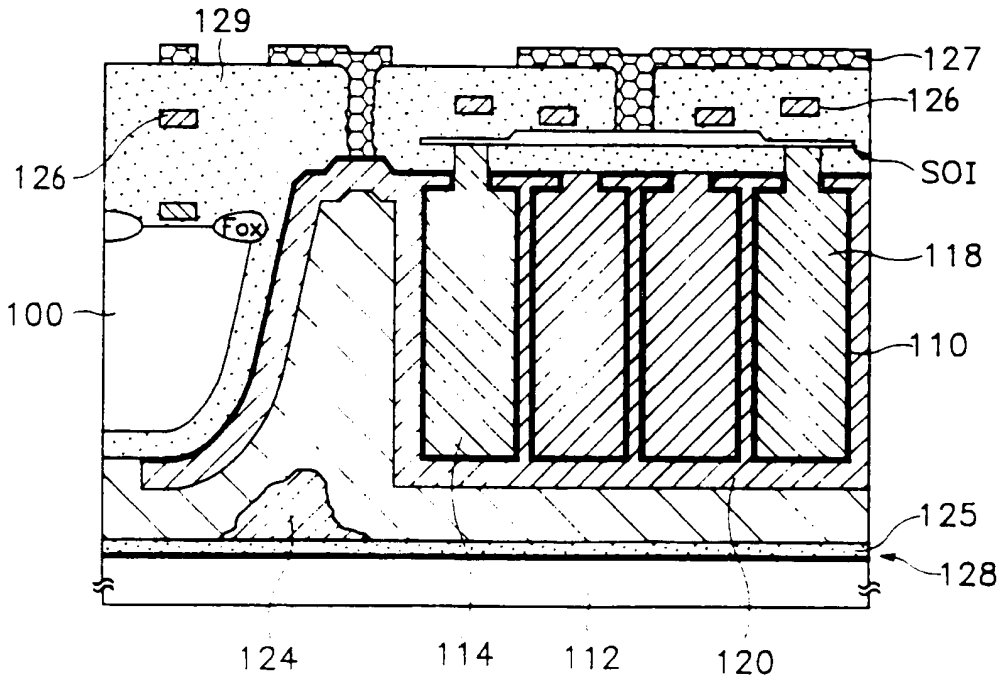
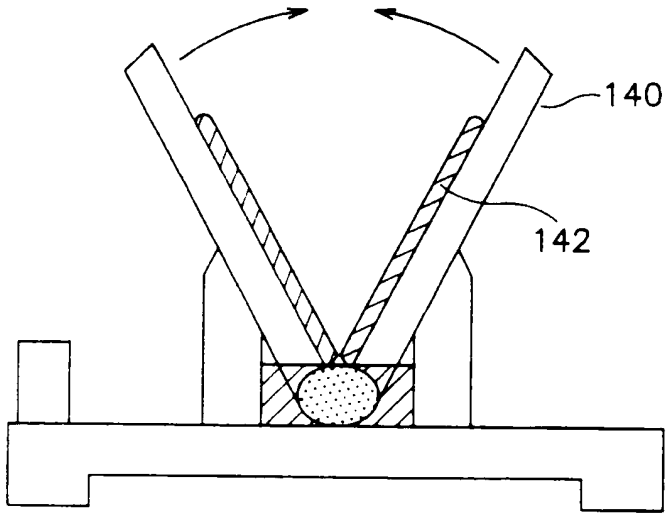


FIG.4



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 31 0488

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	EP-A-0 356 218 (SONY CORP) * the whole document *	1-19	H01L27/108 H01L21/82
A	PATENT ABSTRACTS OF JAPAN vol. 16, no. 347 (E-1240)27 July 1992 & JP-A-04 107 858 (NEC CORP) 9 April 1992 * abstract *	1-19	
A	PATENT ABSTRACTS OF JAPAN vol. 16, no. 564 (E-1295)4 December 1992 & JP-A-04 216 667 (SONY CORP) 6 August 1992 * abstract *	1-19	
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 280 (E-779)(3628) 27 June 1989 & JP-A-01 067 956 (FUJITSU LTD) 14 March 1989 * abstract *	1-19	
A	PATENT ABSTRACTS OF JAPAN vol. 15, no. 448 (E-1133)14 November 1991 & JP-A-03 190 164 (MATSUSHITY ELECTRIC IND CO LTD) 20 August 1991 * abstract *	1-19	TECHNICAL FIELDS SEARCHED (Int.Cl.5) H01L
A	PATENT ABSTRACTS OF JAPAN vol. 17, no. 199 (E-1352)19 April 1993 & JP-A-04 342 166 (MITSUBISHI ELECTRIC CORP) 27 November 1992 * abstract *	1-19	
A	PATENT ABSTRACTS OF JAPAN vol. 15, no. 417 (E-1125)23 October 1991 & JP-A-03 173 175 (HITACHI LTD) 23 October 1991 * abstract *	1-19	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	8 February 1994	Sinemus, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
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